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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,356	10/30/2003	Tony M. Turner	1875.3990001	6728
26111	7590	04/04/2005	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			NGUYEN, TAN	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EC

Office Action Summary

Application No.

10/696,356

Applicant(s)

TURNER ET AL.

Examiner

Tan T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) ____ is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

In claim 2 and claim 4, Applicant claimed the step of testing selected bits of the memory, and defining the initial predetermined time based on the testing. Applicant failed to provide proper antecedent basis for the step of testing and defining the initial predetermined time.

2. Claims 2 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear how the step of testing selected bits of the memory and defining the initial predetermined time based on the testing are performed.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuo et al. (U.S. Patent No. 5,991,201).

Kuo et al. disclosed in Fig 1. a data processing system [20] comprising a voltage generation circuit [27], which includes a charge pump [28] and a voltage divider circuit [29], coupled between a program pulse counter [25], timer circuit [26] (column 15-25) and non-volatile memory [30] (column 2, line 54). The timer circuit [26] is used to

control the duration of each of programming pulses of the series of programming pulses (column 3, lines 28-29). The charge pump circuit [28] has an input connected to a first one of the outputs of timer circuit [26], and an output connected to a memory [30] for providing WORD LINE VOLTAGE signal. The WORD LINE VOLTAGE signal has a selectable duration controlled by the timer circuit [26] (column 3, lines 31-37). Kuo et al. disclosed in Fig 2. the partial block diagram of the memory [30] which includes program latch portion [60] having a comparator [61], a program latch [62], a comparator [63] and a program latch [64] (column 4, lines 42-44). The program latch portion [60] allows the sequence of programming pulses to be ended once the cell has been programmed to the appropriate value (column 5, lines 20-26). In Fig. 4, Kuo et al. showed the WORD LINE VOLTAGE signal [Vw] has constant level during four discrete time periods, in which each of these pulses are generated using pulses width of increasing duration. If the basic pulse width is labeled "P", the first pulse has a pulse width or time duration equal to $P/8$, the second has a pulse width or time duration equal to $P/4$, the third pulse has a pulse width equal to $P/2$, and the fourth pulse has a pulse width of P (column 5, lines 58-65). Kuo et al. discloses that between each programming pulse the comparator and program latches are enabled to sense the states of memory cells. If a cell achieved its correct logic state, its corresponding comparator such as [61] or [63] activates its corresponding reset signal to cease application of any further programming pulses (column 6, lines 42-47). However, for the majority of cells with longer programming times, pulses continue to be applied in increasing duration and magnitude (column 6, lines 55-57). Kuo et al. disclosed in Fig. 6 a flow diagram illustrating the

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programming method of memory [30]. The programming operation starts at step [101] by entering the programming mode. At step [103] the programming pulse voltage and duration are set. At step [104] the program pulses in voltage $[V_D]$ and $[V_{WL}]$ are applied to array [40]. At step [105] the state of the bits to be programmed is compared and if all bits have been successively programmed, the programming is complete. If not, at step [106] the programming latches which are connected to programmed bit cells are reset, but other bit lines remain active for subsequent programming pulses. In a subsequent flow through the loop program pulse voltage and duration is again increased at step [103]. This sequence is repeated until all program bits have been successfully programmed (column 7, lines 12-33).

5. Claims 2 and 4 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tanaka et al. is cited to show a memory device having programming pulses of increased pulse widths (Fig. 32).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
March 25, 2003